TRANSFER OF FABRICATION OF UNIVERSAL MEMS INTEGRATED DUAL-SPRING (UMIDS) PROCESS TO A DISTRIBUTED FABRICATION NETWORK

Contract No. N66001-06-C-0013

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Technical Progress Report

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14. ABSTRACT

Spawar has been developing a process sequence called the "Universal MEMS Integrated Dual-Spring"(UMIDS) for several years. This process has shown promise for the fabrication of extremely sensitive inertial sensor devices. Under this effort, Spawar researchers were tasked with the transfer of the UMIDS process to the DARPA-established MEMS Exchange program at the Corporation for National Research Initiatives (CNRI) in Reston Virginia. Specifically, Spawar provided to the MEMS Exchange the process sequence, device designs, and various process details and parameters to provide a starting point to allow the MEMS Exchange to fabricate accelerators using the UMIDS process. This final report outlines our efforts and the results of the fabrication of the accelerator devices made using the Spawar UMIDS process. The UMIDS process was successfully transferred to the MEMS Exchange.

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Introduction

Spawar has been developing a process sequence called the "Universal MEMS Integrated Dual-Spring" (UMIDS) for several years. This process has shown promise for the fabrication of extremely sensitive inertial sensor devices. Under this effort, Spawar researchers were tasked with the transfer of the UMIDS process to the DARPA-established MEMS Exchange program at the Corporation for National Research Initiatives (CNRI) in Reston Virginia. Specifically, Spawar provided to the MEMS Exchange the process sequence, device designs, and various process details and parameters to provide a starting point to allow the MEMS Exchange to fabricate accelerators using the UMIDS process. The UMIDS process is an extremely challenging process sequence. It is composed of over 30 masking steps, dozens of processing steps, the assembly of multiple processed wafers into a 3-wafer bonded wafer stack, and fabrication of fragile, small-dimensioned mechanical supports for the inertial sensor proof mass. In comparison, most non-IC integrated MEMS devices are less than 8 masks. This report outlines our efforts and results in the fabrication of accelerator devices made using the Spawar UMIDS process. The UMIDS process was successfully transferred to the MEMS Exchange.

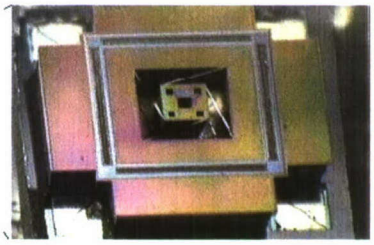


Figure 1: Bonded die of bottom two wafers. The released proof-mass in the center is held by two sets of springs in each corner.

The fabrication was divided into 3 major parts: one fabrication cycle for the top and bottom wafers in the stack, and 2 cycles for the middle wafer.

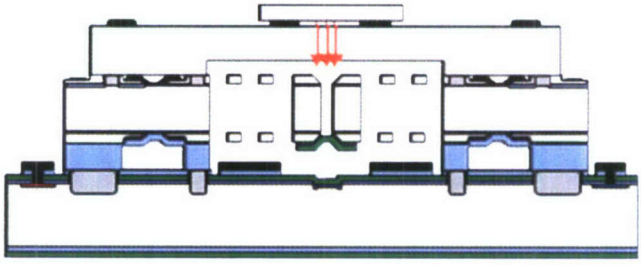


Figure 2: Cross-sectional view of sensor with 3 wafers.

The bottom wafer (also known as the lower-mirror wafer) was fabricated as described in runcard R2737. The fabrication sequence consists of 7 masks and 5 wafers. The main objective was to fabricate diodes which are used to read the optical signal that is modified by moving proof-mass. The diodes are successfully fabricated and measured. See Appendix 1 for results as reported by Spawar.

The middle wafer fabrication is and has been one of the most complicated MEMS fabrication sequences attempted. Unlike standard SOI wafers, the starting substrate in this fabrication is custom made to have buried-oxide (BOX) and silicon device layers on both sides of the handle substrate. Due to this unique feature of the wafers, the wafer supplier (which was contracted by Spawar before the project was awarded) spent significant resources to make wafers with acceptable tolerances and defect density. Unfortunately, despite all their development efforts, the wafers were still not as good as standard SOI wafers and have significant defects on the BOX layer on the designated backside.

The middle wafers (also known as upper-mirror wafers) were fabricated in two cycles in runcards R2739 (cycle 1-part 1), R3486 (cycle 1- part2), R3948 (cycle 2-part 1) and R3947 (cycle 2- part2). The fabrication sequence consists of 13 masks, and 4 device wafers. The first cycle was completed with partial success. Of two DRIE tools used in the first cycle, neither had the low-frequency option that is necessary to minimize the so-called footing effect. In particular, the PM1 chamber on the Unaxis tool has significant non-uniformity between the wafers, especially between the standard silicon and SOI wafers. Unfortunately, one of the key etches that ended on the BOX was performed on the PM1 before it was realized that this was not a suitable tool and process for SOI wafers. The key problem was that the number of available custom SOI wafers provided for the run was only 4 and we could not afford to perform destructive testing as we did not know what we needed in the subsequent steps. Therefore all testing for the etches was performed using standard silicon wafers. Later, it turned out that the testing done on the standard wafers was not representative for what happens on the device wafers. The DRIE in the device layer etches had a re-entrant profile. In addition, handle etches in PM1 resulted in major grass formation, which in turn, stalled the etch. We had to perform multiple isotropic etches to clean off the grass and restart the etches. When we finally managed to etch one of the device wafers completely, we realized that the complicated DRIE/RIE on the handle etch and the nature of the etch on the device layer resulted in major damage on the support beams. The last device wafer had the same problems.

The second cycle in the fabrication of the middle wafers was much improved. Nevertheless, in the second of the two-step KOH patterning steps, the non-uniformity in thickness of the device layers and the quality of the BOX interface caused two critical problems. The more critical of these problems resulted in residual silicon on one side of the wafers, while the other side (front) was over-etched. When over-etched, the defects in the BOX causes pit formation underneath the BOX into the handle wafer. At that point, we stopped the KOH etch. The fabrication resumed with multi-layer AR coatings and with the Al metal contact formation. Soon after the metal pads are formed, during electrical testing it was realized that although everything worked as expected

on the frontside, the backside pads were not electrically isolated. After weeks of investigation, we concluded that this electrical path was provided by residual silicon which was thought to be etched completely. The easiest solution to achieve the electrical isolation is by using an extra mask and dry-etching away that residual path between the pads. This critical two-sided DRIE step was done on our upgraded 6" STS tool, which is now a dual frequency system, instead of using the two single-frequency DRIE tools.

Finally, the top wafer (also known as the capping wafer) was fabricated in runcard R2745. There have been significantly different versions of the fabrication sequences proposed. First, and the more complicated version, is based on a silicon substrate and consisted of 11 masks and 5 wafers. The second and simpler version had only 3 masks and was based on UV-grade fused-silica glass and anti-reflective (AR) coatings on both sides. The fabrication was a partial success, as there were some dies lost during metal patterning. We observed some discoloration on the AR coating during metal patterning which suggests that those areas will not perform the same as the unaffected areas.

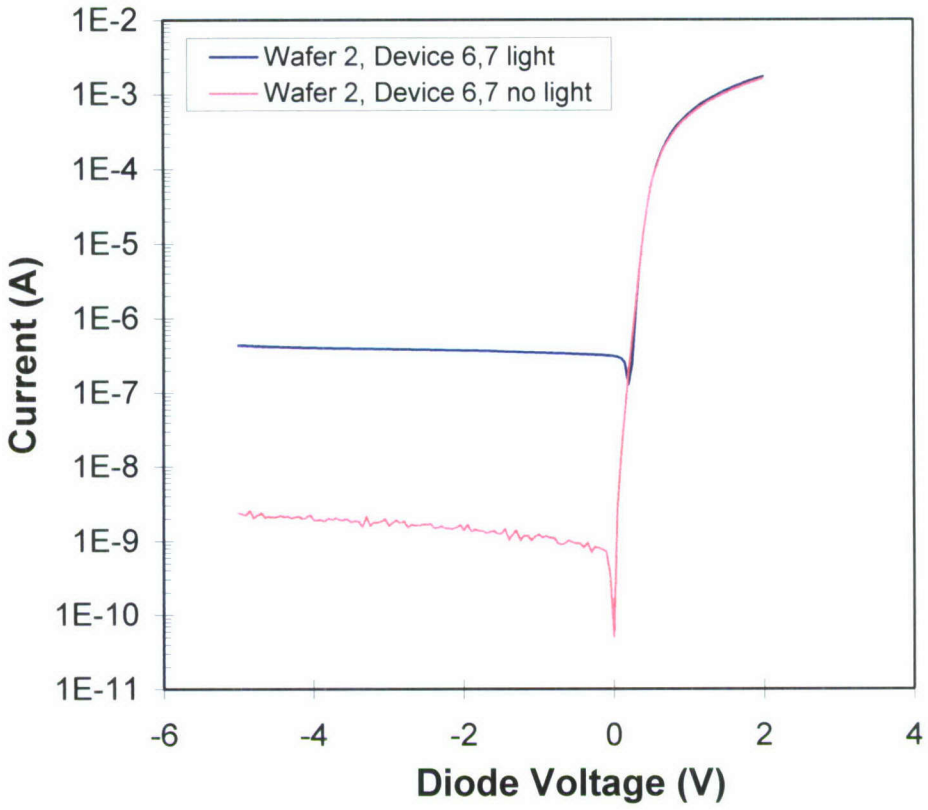
In conclusion we have fabricated the three wafers needed to form the three-wafer stack for the sensor. The first bond between the bottom and middle wafer is done using glass-frit 450C and the top wafer is bonded at 300C using a Au/Sn layer.

APPENDIX 1

Measurement of diodes on the lower mirror wafer. All electrical metrology has been performed by SPAWAR.

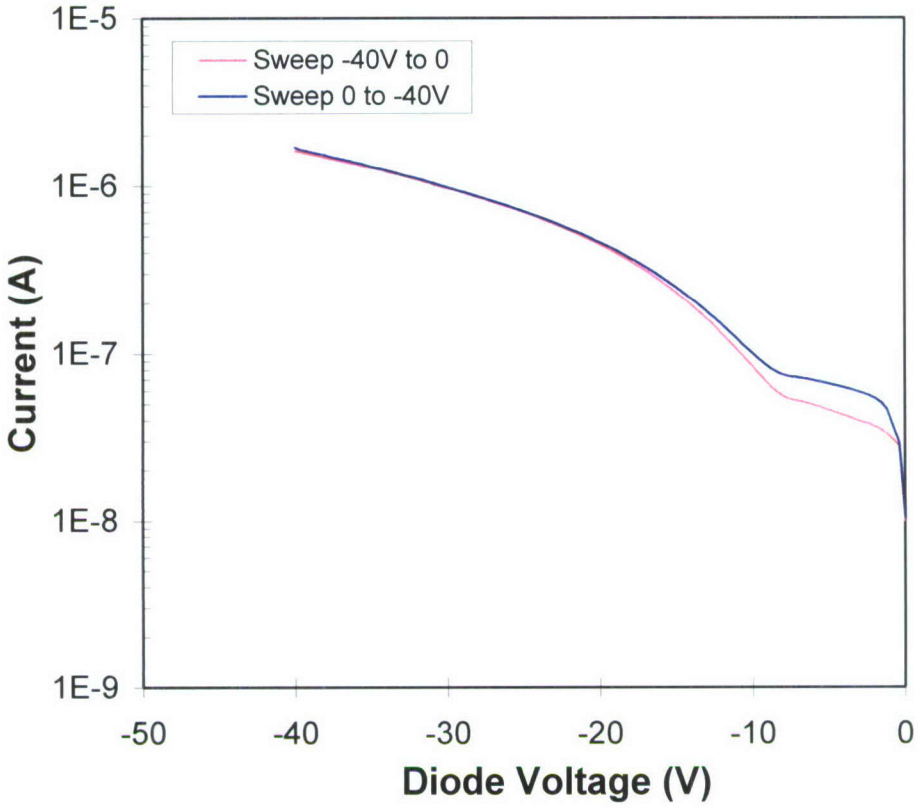
	ideality	std	Rs (KΩ)	std (KΩ)	Is (Vr=1) no light (nA)	std (nA)	Is (Vr=1) w/ light (nA)	std (nA)
wafer 1	1.85	0.12	5.11	3.81	21.50	8.83	391.17	25.90
wafer 2	1.84	0.12	2.31	1.16	18.74	26.64	389.33	43.60
wafer 3	1.87	0.09	1.80	1.73	10.44	9.11	344.60	11.93
wafer 4	1.91	0.13	6.68	8.36	20.18	14.51	403.80	50.97
wafer 5	1.77	0.11	1.37	0.70	12.38	1.57	348.60	4.51
wafer 6	1.66	0.18	1.68	1.51	23.30	20.94	383.17	21.66
wafer 7	1.57	0.30	2.34	2.71	16.30	10.39	380.20	24.68
avr	1.78		3.04		17.55		377.27	
std	0.12		2.03		4.76		22.27	

The plot below representss one of the best diodes characterized. It has a leakage current of just over 1 nA at a reverse bias of 1 volt. On-Resistance and ideality are causes for concern on all diodes. No Schotky barrier was observed on any of the diodes measured.

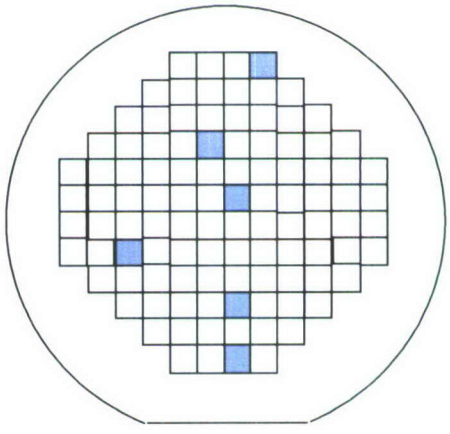


Charging effects were observed resulting in hysterisis.

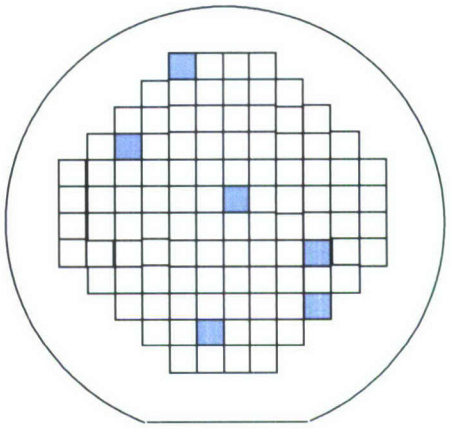
Leakage currents increased significantly beyond 10 volts reverse bias.



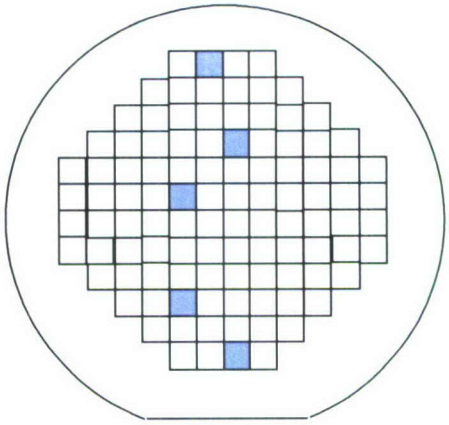
Wafer #1 Location	ideality	Rs (KW)	Is (V=-1) no light (nA)	Is (V=-1) w/ light (nA)
1,4	1.91	6.98	31.60	431.00
4,5	1.85	1.45	13.70	366.00
6,7	1.82	1.51	12.80	370.00
8,3	1.77	4.28	21.10	379.00
10,5	1.72	4.86	16.90	387.00
12,3	2.06	11.60	32.90	414.00
avr	1.85	5.11	21.50	391.17
std	0.12	3.81	8.83	25.90



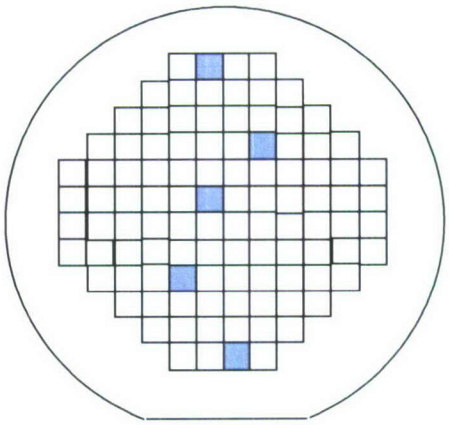
Wafer #2 Location	ideality	Rs (KW)	Is (V=-1) no light (nA)	Is (V=-1) w/ light (nA)
1,1	1.70	3.50	66.70	473.00
4,2	2.04	1.55	34.20	400.00
6,7	1.75	0.85	1.70	356.00
8,10	1.89	1.79	2.52	371.00
10,8	1.84	3.83	3.45	364.00
11,3	1.82	2.33	3.88	372.00
avr	1.84	2.31	18.74	389.33
std	0.12	1.16	26.64	43.60



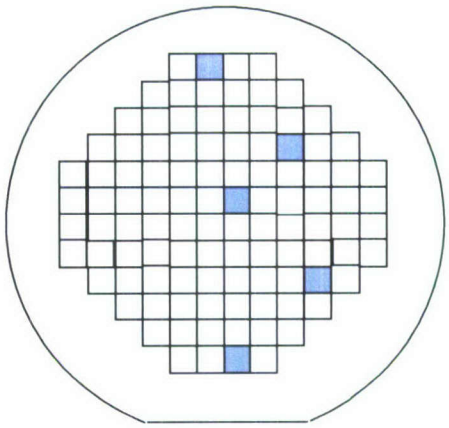
Wafer #3 Location	ideality	Rs (KW)	Is (V=-1) no light (nA)	Is (V=-1) w/ light (nA)
1,2	1.91	1.45	8.77	348.00
4,6	1.80	0.53	2.81	332.00
6,5	1.74	0.48	2.14	343.00
10,3	1.94	1.81	14.40	337.00
12,3	1.96	4.71	24.10	363.00
avr	1.87	1.80	10.44	344.60
std	0.09	1.73	9.11	11.93



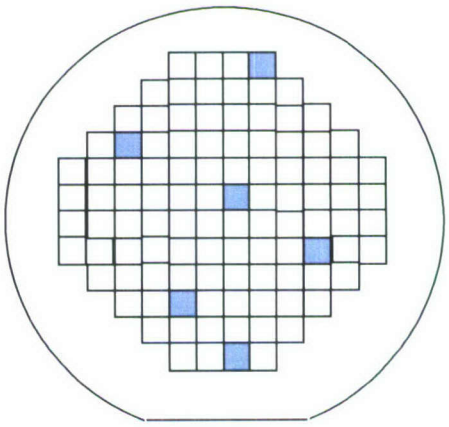
Wafer #4 Location	ideality	Rs (KW)	Is (V=-1) no light (nA)	Is (V=-1) w/ light (nA)
1,2	1.87	3.69	16.70	410.00
4,7	1.89	1.30	12.70	371.00
6,6	1.82	1.49	11.50	380.00
9,4	1.84	5.62	14.10	368.00
12,3	2.14	21.30	45.90	490.00
avr	1.91	6.68	20.18	403.80
std	0.13	8.36	14.51	50.97



Wafer #5 Location	ideality	Rs (KW)	Is (V=-1) no light (nA)	Is (V=-1) w/ light (nA)
1,2	1.74	2.39	15.00	347.00
4,8	1.92	1.47	12.70	344.00
6,7	1.62	0.60	11.30	356.00
9,9	1.79	0.84	11.40	347.00
12,3	1.77	1.56	11.50	349.00
avr	1.77	1.37	12.38	348.60
std	0.11	0.70	1.57	4.51



Wafer #6 Location	ideality	Rs (KW)	Is (V=-1) no light (nA)	Is (V=-1) w/ light (nA)
1,4	1.82	2.82	21.10	387.00
4,2	1.79	0.65	13.70	376.00
6,7	1.35	0.60	11.20	375.00
8,10	1.62	0.65	65.40	425.00
10,3	1.62	1.15	11.80	367.00
12,3	1.77	4.23	16.60	369.00
avr	1.66	1.68	23.30	383.17
std	0.18	1.51	20.94	21.66



Wafer #7 Location	ideality	Rs (KW)	Is (V=-1) no light (nA)	Is (V=-1) w/ light (nA)
2,4	1.58	0.62	11.00	370.00
4,2	1.28	0.62	10.70	367.00
6,7	1.29	0.57	10.90	382.00
9,5	1.70	3.08	14.20	360.00
11,4	2.01	6.80	34.70	422.00
avr	1.57	2.34	16.30	380.20
std	0.30	2.71	10.39	24.68